while the restriction requirement was not of the "explicit" kind, it was technically in force as a matter of "original presentation." The Applicants respectfully disagree with the restriction requirement, as will be shown hereinbelow. Therefore, the Applicants maintain traversal of the restriction requirement for the reasons given in the Responses filed with the Office on October 15, 2002 and November 26, 2002, and request reconsideration thereof.

Given the request for reconsideration, the right to file a petition under 37 C.F.R. § 1.144 is preserved herein. If the Examiner continues to believe that the remarks offered in the past Responses and herein are non-responsive to the previously-mailed Office Actions, the Applicants respectfully request that this Supplemental Response also be expressly considered as a Petition from Requirement for Restriction under 37 C.F.R. § 1.144. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Response to Restriction Requirement

The Office Action Summary asserts that the Response filed on October 15, 2002 was non-responsive, since it presented only claims drawn to a non-elected invention. The Examiner expressed similar concerns with respect to the Response filed on November 26, 2002, during the telephone conference referenced above. The Applicants respectfully disagree, and maintain that the pending claims, especially including specifically elected and amended original claim 10, are not directed toward a separate and distinct invention from those embodiments addressed by claims 1-20 as originally filed.

A. Currently-Pending Claim 10 is Not a Separate and Distinct Invention

In the Application as originally filed, claims 9 and 10 read:

> 9. A method comprising:
> storing programmed code on a computer readable medium external to a processor;
> executing, by the processor, the programmed code; and
> controlling one or more functions of the processor in response to executing the programmed code.

10. The method of claim 9 wherein the one or more functions are controlled by directly triggering hardware on the processor in response to executing the programmed code.

In the first Office Action Response, claim 9 was cancelled and claim 10 was amended to incorporate the limitations of claim 9 so as to appear in independent form, thus:

10. (Once Amended) [The method of claim 9] A method comprising:
storing programmed code on a computer readable medium external to a processor;
executing, by the processor, the programmed code; and
controlling one or more functions of the processor in response to executing the programmed code, wherein the one or more functions are controlled by directly triggering hardware on the processor in response to executing the programmed code.

In essence, claim 10 remained unchanged. All of the limitations in place as of the original filing were present after the amendment. Claim 10 was amended once more, in the Response of November 26, 2002 to incorporate an additional limitation. Thus:

10. (Twice Amended) A method comprising:
storing programmed code on a computer readable medium external to a processor;
executing, by the processor, the programmed code; and
controlling one or more functions of the processor in response to executing the programmed code, wherein the one or more functions are controlled by updating at least one machine specific register associated with a logic unit of the processor and by directly triggering hardware on the processor in response to executing the programmed code.

This is the current form of claim 10. All of the limitations present as of the original Application filing are still in place. A single limitation has been added. The invention claimed is therefore not "separate and distinct", but is in fact a more limited version of that embodied in an originally-filed claim. Therefore, claim 10 as amended and elected is not a separate invention and the Applicants respectfully request reconsideration and withdrawal of the restriction requirement with respect to claim 10.

B. Currently-Pending Claims 21-40 are Not a "Separate and Distinct" Invention

Currently-pending claims 21-40 were added as part of the first Office Action Response in this matter. As noted above, it has been asserted that claims 21-40 have been withdrawn by the Office from consideration, because embodiments of the invention claimed therein are distinctly different from those claimed in original claims 1-20, as a matter of "original presentation." The Applicants respectfully disagree for the following reasons.

As noted in a previous Response, the originally-filled Application reads as follows:

> "In an example embodiment, **the firmware code 210 implements microcode operations using registers which are specific to a particular machine or to a particular model of a machine. The registers are referred to herein as "Machine Specific Registers."** The machine specific registers function as an interface between the firmware 206 and the processor 204. ... In the example embodiment shown in FIG. 2A, processor 204 includes a plurality of machine specific registers (MSRs) 208. In one embodiment, **one or more of the MSRs 208 are associated with one or more functional units of the processor 204."** (Application, pg. 4, line 29 - pg. 5, line 8.)

It was also noted that originally-filed claims 5, 6, 7, and 11 (now cancelled) read as follows:

> 5. The computer system of claim 1 wherein the processor further comprises **a plurality of registers associated with one or more functional units of the processor.**
>
> 6. The computer system of claim 5 wherein **the instructions implement microcode functions by updating one or more of the plurality of registers.**
>
> 7. The computer system of claim 5 wherein **the instructions implement microcode functions by reading one or more of the plurality of registers.**
>
> 11. The method of claim 9 wherein the **one or more functions are controlled by updating one or more registers associated with a logic unit** on the processor in response to executing the programmed code

It should specifically be observed that claim 11 depends from originally-filed claim 9, which has been incorporated into claim 10, as noted above.

Finally, it was noted that in addition to these recited claims, several other originally-filed claims also address the use of a register associated with a functional unit of the microprocessor,

defined in the Application as a "machine specific register." For example, original claims 18 and 19 are shown below:

18. A processor comprising:
a plurality of logic units; and
one or more registers associated with each one of the plurality of logic units, the one or more registers to trigger processor hardware logic functions when one of the registers is updated in response to an external microcode instruction.

19. The processor of claim 18 **wherein one or more of the registers are associated with two or more of the logic units.**

Thus, a distinct and specific error in the restriction requirement arises because the term "machine specific register" has been defined as a synonym for registers associated with processor functional units in the original Application. Such "registers associated with processor functional units" have been listed several times as elements in original claims 1-20, and are re-listed in synonymous form as "machine specific registers" in claims 21-40 for purposes of descriptive consistency and economy. Therefore, the embodiments in claims 21-40, listing machine specific registers, are not distinctly different inventions from the embodiments in claims 1-20, listing registers associated with processor functional units. Any search made which included such associated registers should have included machine specific registers, since they are the same thing. At this time, the Applicants again respectfully request reconsideration and withdrawal of the restriction requirement as noted in M.P.E.P. § 821.01.

CONCLUSION

The Applicants respectfully request reconsideration and withdrawal of the restriction requirement, petition from the Requirement for Restriction, if necessary, and submit that claims 10 and 21-40 are in condition for allowance. The Examiner is invited to telephone the Applicants' attorney, Mark Muller, at (210) 308-5677, or the undersigned, to facilitate prosecution of this Application, of if he has any questions whatsoever. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

HOWARD CHIN ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 349-9592

Date Jan. 24, 2003 By Ann M. McCrackin
Ann M. McCrackin
Reg. No. 42,858

I hereby certify that this paper is being transmitted by facsimile to the U.S. Patent and Trademark Office on the date shown below.

Jane E. Sagers

January 24, 2003.
Date of Transmission

APPENDIX I
Clean Version of Pending Claims

EXTERNAL MICROCODE
Applicant: Howard Chin et al.
Serial No.: 09/476,622

01

10. A method comprising:

storing programmed code on a computer readable medium external to a processor;

executing, by the processor, the programmed code; and

controlling one or more functions of the processor in response to executing the programmed code, wherein the one or more functions are controlled by updating at least one machine specific register associated with a logic unit of the processor and by directly triggering hardware on the processor in response to executing the programmed code.

02

21. A system, comprising:

a bus;

a processor including a plurality of machine specific registers, wherein each one of the plurality of machine specific registers is associated with one or more functional units of the processor; and

a computer readable medium external to the processor and coupled to the processor by the bus, the computer readable medium to store instructions to implement microcode functions which result in changing a value of at least one bit in at least one of the plurality of machine specific registers.

22. The system of claim 1, wherein the computer readable medium is firmware.

23. The system of claim 1, wherein the plurality of machine specific registers includes a bank of registers associated with one of the functional units.

24. The system of claim 1, wherein one of the functional units is an internal bus controller.

25. The system of claim 1, wherein one of the functional units is an internal data cache of the processor.

26. The system of claim 25, wherein the instructions implement microcode functions by updating the at least one of the plurality of machine specific registers.

27. The system of claim 26, wherein the instructions implement microcode functions by setting the at least one bit to invalidate a line of the cache.

28. The system of claim 25, wherein the instructions implement microcode functions by triggering processor hardware logic and by manipulating the plurality of machine specific registers.

29. A method, comprising:

storing microcode on a computer readable medium external to a processor;

executing the microcode using the processor, wherein the processor includes a plurality of machine specific registers associated with at least two functional units of the processor; and

controlling one of the at least two functional units of the processor in response to executing the microcode by modifying a value of at least one bit included in one of the plurality of machine specific registers.

30. The method of claim 29, wherein modifying a value of at least one bit included in one of the plurality of machine specific registers associated with one of the at least two functional units of the processor operates to affect the behavior of an other one of the at least two functional units of the processor.

31. The method of claim 29, wherein a logical source register and a logical destination register for executing an instruction of the microcode are selected from the plurality of machine

specific registers.

32. The method of claim 29, wherein the at least two functional units are linked by a communication bus to a data control unit to fetch an instruction of the microcode from the computer readable medium external to a processor.

33. The method of claim 29, wherein controlling one of the at least two functional units of the processor in response to executing the microcode further includes:

controlling a non-performance critical function.

34. The method of claim 33, wherein the non-performance critical function is selected from the group consisting of:

cache flushing, cache invalidation, setting processor features, reading processor features, machine check handling, floating point calculations, processor diagnosis, architecture handling for backward compatibility, authentication, platform management interrupt, diagnostic functions and debug functions.

35. An article comprising a machine-accessible medium having associated data, wherein the data, when accessed, results in a machine performing:

storing microcode in firmware external to a processor;

executing the microcode by the processor;

updating one or more machine specific registers associated with a logic unit on the processor in response to the executing of the programmed code; and

controlling one or more functions of the logic unit on the processor based on a value stored in the one or more machine specific registers.

36. The article of claim 35, wherein the machine-accessible medium further includes data, which when accessed by the machine, results in the machine performing:

moving a value from a general purpose register of the processor to th one or more machine specific registers.

D2

37. The article of claim 35, wherein the machine-accessible medium further includes data, which when accessed by the machine, results in the machine performing:

reprogramming the microcode in the firmware.

38. An apparatus, comprising:

a first logic unit; and

at least two machine specific registers associated with the logic unit, the at least two machine specific registers to trigger processor hardware logic functions when a selected one of the at least two machine specific registers is updated in response to executing a microcode instruction fetched from a memory external to the processor.

39. The apparatus of claim 38, further comprising:

a second logic unit associated with a selected one of the at least two machine specific registers.

40. The apparatus of claim 39, wherein changing a value of at least one bit in a selected other one of the at least two machine specific registers affects the behavior of the second logic unit.